Bounds on the VLSI Layout Complexity of Homogeneous Product Networks

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Abstract

In this paper we obtain bounds on the area and wire length required by VLSI layouts of homogeneous product networks with any number of dimensions. The lower bounds are obtained by computing lower bounds on the bisection width and the crossing number. The upper bounds are derived by using traditional frameworks like separators and bifurcators, as well as a new method based on combining collinear layouts. This last method has led to the best area and wire lengths for most of the homogeneous product networks we considered.

1: Introduction

The cross product is a well known operation defined on graphs. When applied to interconnection networks, the cross product operation combines a set of "factor" networks into a *product network*. Several well known networks are instances of product networks, including the grid, the torus, and the hypercube. A product network is said to be *homogeneous* if all its factor networks are isomorphic. Otherwise the product network is *heterogeneous*. All the above examples of product networks are homogeneous and others have been recently introduced. However, there is no paper which studies the VLSI complexity of product networks as a general class. This paper makes an attempt to fill this gap.

In this paper we obtain bounds on the area and the wire length required by VLSI layouts of homogeneous product networks. These are the two most important parameters of a layout, since a large area implies low yield in the fabrication process and long wires imply large communication delays (see [10] for the technological details). The VLSI model assumed in this paper is the Thompson's model [9] where the VLSI layout area is seen as a two dimensional grid into which the network has to be embedded.

We start our study by defining a new intrinsic parameter of any connected graph, which we call the *maximal congestion*. From the maximal congestion of the factor graph we are able to obtain lower bounds on the area and wire length of the product network. Subsequently, we obtain upper bounds for product networks with bounded degree by using two traditional frameworks: *separators* and *bifurcators*. Finally, we present a universally applicable method to obtain efficient layouts based on collinear layouts (layouts with all the nodes in a line). Briefly, we combine collinear layouts for the factor network to obtain a layout for the product.

We applied all these approaches to several of the well-known networks as well as to others not previously introduced in the literature. The results show that the method

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based on collinear layouts yields optimal area layout in most of the cases. The separator approach also obtains optimal area layouts in some cases when efficient bisectors for the factor network are known. The bifurcator approach does not generate optimal area layouts as often as the others but its layouts are larger only by a polylogarithmic factor of the size of the factor graph. For the maximum wire lengths, the method based on collinear layouts generates optimal layouts in many cases if the number of dimensions is bounded. When the layouts are not optimal their bounds are tighter than those of the other methods.

Due to space limitations some of the proofs in this paper have been shortened. For a full version of those proofs we refer the reader to [4].

2: Definitions

We start by defining the class of product graphs considered in this paper.

Definition 1 *The r-dimensional product graph, denoted as PG_r, of a graph G is the graph whose vertices comprise all the r-tuples $x = x_r x_{r-1} ... x_2 x_1$ such that every x_i, $1 \leq i \leq r$, is a vertex of G, and whose edges comprise all the pairs of vertices (x, y) such that x and y differ in exactly one index position i and (x_i, y_i) is an edge of G.*

The number of nodes of G is denoted as N. Therefore, PG_r has N^r nodes. The diameter of G is denoted as d and its maximum vertex degree is denoted as Δ. The vertex degree of a node u is denoted as Δ_u.

Next we need to define several properties of networks which will be used in this paper.

Definition 2 *The maximal congestion of a graph G is the congestion of any embedding of the N-node* directed *complete graph onto G.*

Upper bounds on the maximal congestion have been used as intermediate values to obtain lower bounds on the bisection width and crossing number of graphs [5, 6]. However, the maximal congestion has not been previously identified as a parameter of a graph.

The bisection width of a graph is the minimum number of edges that have to be removed from it to obtain two disjoint subgraphs with the same number of nodes (within one). The crossing number of a graph is the minimum number of edge crossings of any drawing of the graph in the plane. These last two properties have been traditionally used to obtain lower bounds on the layout area of a graph.

We continue by defining the class of separators used in this paper.

Definition 3 *Let $f(x)$ be a monotonically nondecreasing function. G has a $f(x)$-bisector either if it has only one node or if by removing at most $f(N)$ edges it can be divided into two subgraphs with the same number of nodes (within one), both with $f(x)$-bisectors.*

In general, separators need not bisect the graph at each stage. Our definition is more restrictive, for instance, than the definition of separator used by Leiserson [7]. However, Ullman [10] shows how to obtain a bisector (strong separator) from a separator defined by Leiserson. We will now define the concept of bifurcator.

Definition 4 *A graph G has a F-bifurcator either if it has only one node or if by removing at most F of its edges it can be divided into two subgraphs, both with $F/\sqrt{2}$-bifurcators.*

The VLSI layout model used was defined by Thompson [9], and considers the layout area as being divided into square "tiles" of unit area, placed in a grid fashion. Each tile can hold either a section of wire, a node, or a wire crossing. The wires of the layout run either horizontally or vertically on this grid. If two wires enter the same tile they must have different directions and they cannot change direction in the tile.

When a node has a degree larger than 4, Thompson proposed to model it with a set of adjacent tiles whose perimeter is at least the desired degree. Although the smallest area

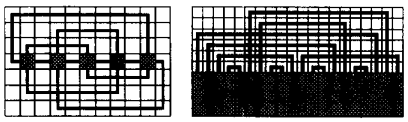

Figure 1: (a) Collinear layout for K_5. (b) Normal collinear layout for K_5.

required to have a perimeter of Δ_u for a node u has $O(\Delta_u)$ tiles, it is much more realistic to assume that a node with vertex degree Δ_u will require area at least $\Omega(\Delta_u) \times \Omega(\Delta_u)$. In this paper we shall assume that any node u is laid out as a rectangle with sides of length at least $\Omega(\Delta_u)$.

Under this model the *length of a wire* is the number of tiles traversed by the wire from its source node to its destination node. For technological reasons, the *layout area* is defined as the area of the smallest rectangle that contains all the allocated tiles of the layout. This value is fully described with the length and the width of this rectangle. In this paper the *width* of a layout is assumed to be the length of the shorter side of the rectangle and the *length* of the layout is the length of the longer side. We also assume that the rectangle is oriented in the grid with the longer side horizontally placed. Figure 1.(a) shows an example of layout for K_5, the 5-node complete graph, where all the nodes are placed in a horizontal line. This kind of layout is called a *collinear layout*. This layout has width 7, length 11, layout area 77, and length of the longest wire 15.

in Section 4.3 we use collinear layouts of the factor graph to generate layouts for the product graph. To be able to use them, we impose several restrictions to the collinear layouts. We assume that the nodes are horizontally aligned.

Definition 5 *A collinear layout is* seminormal *if all the nodes in the layout are placed at the bottom rows of the layout, a node u occupies Δ rows and Δ_u columns, and all the wires are laid down above the row Δ.*

Definition 6 *A collinear layout is* normal *if it is seminormal, all the nodes are touching, and all the wires are laid down as two vertical sections connected by a horizontal section.*

For the above classes of layouts we define a new parameter, the *wiring width*, that is the number of rows used to route the wires in the layout. Figure 1.(b) presents a normal collinear layout for K_5 with wiring width of 6.

3: Lower bounds

In this section we obtain lower bounds on the layout area and wire length required by any layout of PG_r. We recall from [3] that if the maximal congestion of G is k, then the maximal congestion of PG_r is at most kN^{r-1} and the bisection width is at least $\frac{N^{r+1}}{2k}$. Note that it is not possible to obtain a similar result by just knowing the bisection width of G. In this sense, the maximal congestion carries more information than the bisection width.

Lemma 1 *If G has E edges and maximal congestion of k, then the crossing number of PG_r is at least $\frac{(N^r-1)(N^r-2)(N^r-3)}{20k^2N^{r-2}} - \frac{rEN^{r-1}}{2}$*

Proof: It is shown in [8] that if an arbitrary graph G has E edges and maximal congestion of k then its crossing number is at least $\frac{N(N-1)(N-2)(N-3)}{20k^2} - \frac{E}{2}$. Since the maximal congestion of PG_r is at most kN^{r-1} and it has rEN^{r-1} edges [3], we obtain the claimed

lower bound. ∎

In [9], Thompson showed that the square of the bisection width is a lower bound (within a constant factor) on the layout area required by any layout of a graph. Similarly, Leighton [5] presented the crossing number as a lower bound on the layout area of any layout of a graph. Hence, the following theorem.

Theorem 1 *If the maximal congestion of G is k, then the layout area of PG_r is at least $\Omega(\frac{N^{2(r+1)}}{k^2})$.*

Now we present a lower bound on the length of the longest wire.

Theorem 2 *If the maximal congestion of G is k and its diameter is d, then the length of the longest wire in any layout of PG_r is at least $\Omega(\frac{N^{r+1}}{krd})$.*

Proof: Theorem 5-2 in [5] shows that any layout of a graph with diameter D and minimum layout area A has some wire of length at least $A^{1/2}/3D$. The diameter of PG_r is rd [3], and from Theorem 1 its layout area is at least $\Omega(\frac{N^{2(r+1)}}{k^2})$. Therefore, we can conclude that any layout of PG_r has some wire of length at least $\frac{\Omega(N^{r+1}/k)}{3rd} = \Omega(\frac{N^{r+1}}{krd})$. ∎

4: Upper bounds

In this section we first present upper bounds obtained by traditional frameworks, namely bisectors and bifurcators. Since these frameworks are only applicable to networks with bounded vertex degree, we will assume that G has bounded vertex degree and that r is also bounded. Subsequently, we present another approach that has no restriction on the vertex degree or the number of dimensions. This method is based on the existence of efficient collinear layouts for the factor networks.

4.1: Upper bounds based on bisectors

The following theorem is the basic result of this section.

Theorem 3 *If G has a $f(x)$-bisector then PG_r has a $O(x^{(r-1)}f(x))$-bisector.*

Proof: (Sketch) The proof shows how to divide PG_r into 2^r disjoint subgraphs, each being the product of r graphs with $\lfloor N/2 \rfloor$ nodes and $f(x)$-bisectors, and eventually, some isolated nodes. This process is done in r bisection steps, each of which cuts $O(N^{r-1}f(N))$ edges from its corresponding graph. The partition process applied to PG_r can be also applied to each of the obtained subgraphs, and so on, until all the nodes are isolated. ∎

Once we obtain a bisector for product networks we are ready to apply it to obtain bounds on the layout parameters.

Theorem 4 *If G has a $f(x)$-bisector then PG_r can be laid out in a square of side $O(Nf(N)\log N)$ when $r = 2$, or side $O(N^{(r-1)}f(N))$ when $r > 2$.*

Proof: Theorem 3.5 in [10] states that any n-node graph with a $g(x)$-bisector and bounded degree can be laid out in a square of side $O(max(\sqrt{n}, \sum_{i=0}^{\log_4 n} 2^i g(n/4^i)))$. PG_r has N^r nodes and, from Theorem 3, has a $O(x^{(r-1)/r}f(x^{1/r}))$-bisector. We can obtain the value of the summation as $\sum_{i=0}^{r\log_4 N} 2^i O((N^r/4^i)^{(r-1)/r} f(N/4^{i/r})) = O(f(N)\sum_{i=0}^{r\log_4 N} 2^i(\frac{N^r}{4^i})^{(r-1)/r})$ since $f(x)$ is a monotonically nondecreasing function. The value of this last summation is $O(N\log N)$ when $r = 2$, or $O(N^{r-1})$ when $r > 2$ [10]. Therefore, the value of the first summation is $O(Nf(N)\log N)$ when $r = 2$, or $O(N^{r-1}f(N))$ when $r > 2$, as claimed. ∎

The most studied kind of bisectors has been those with $f(x) = O(x^\alpha)$, for bounded α. The results of [7] imply that a n-node graph with a $O(x^\alpha)$-bisector can be laid out in area $O(n)$ when $\alpha < 1/2$, in area $O(n\log^2 n)$ when $\alpha = 1/2$, and in area $O(n^{2\alpha})$ when

$\alpha > 1/2$. These upper bounds can be reached with maximum wire lengths of $O(\sqrt{n}/\log n)$, $O(n \log n/\log\log n)$, and $O(n^\alpha)$, respectively [2]. Therefore,

Corollary 1 *If G has a $O(x^\alpha)$-bisector, for bounded α, then PG_r can be laid out in an area of $O(N^2 \log^2 N)$ with maximum wire length $O(N \log N/\log\log N^r)$ when $\alpha = 0$ and $r = 2$, or in an area of $O(N^{2(r+\alpha-1)})$ with maximum wire length $O(N^{r+\alpha-1})$ otherwise.*

4.2: Upper bounds based on bifurcators

The following theorem presents the main result of this section.

Theorem 5 *If G has a F-bifurcator then PG_r has a $N^{r-1}6(2+\sqrt{2})F$-bifurcator.*

Proof: (Sketch) From Theorem 6 in [1] we know that if G has a F-bifurcator then it has a $H = 6(2+\sqrt{2})F$-bifurcator (balanced bifurcator) that bisects the graph at each division. Then, after at most $\log N + 1$ divisions G is transformed into N isolated nodes.

The proof is very similar to the proof of Theorem 3. We show that given PG_r we can obtain 2^r subgraphs each being the product of r graphs with $H/\sqrt{2}$-bifurcators and at most $\lceil N/2 \rceil$ nodes. ∎

We recall here that if G can be laid out in an area A it has a $\sqrt{A}$-bifurcator [1], and hence PG_r has a $N^{r-1}6(2+\sqrt{2})\sqrt{A}$-bifurcator. From Theorem 5 we can obtain bifurcator-based bounds for the area and maximum wire length by using the results from Bhatt and Leighton [1].

Corollary 2 *If G has a F-bifurcator then PG_r can be laid out in an area of $O(N^{2(r-1)}F^2 \log^2(N/F))$ with maximum wire length $O(N^{r-1}F\frac{\log(N/F)}{\log\log(N/6(2+\sqrt{2})F)})$.*

4.3: Upper bounds based on collinear layouts

Here we present another approach, which does not restrict the degree or the number of dimensions. We need a normal collinear layout for G.

4.3.1: Methods for obtaining normal collinear layouts: We are interested in obtaining normal collinear layouts with small wiring width and short wires, because these are the properties that influence the characteristics of the layout of the product graph.

First, observe that any graph G has a normal collinear layout of wiring width at most $\frac{1}{2}\sum_{u \in V} \Delta_u$, where V is the set of nodes of G, since this is the number of wires in the layout and each wire requires no more than one row.

Similarly, if there is an embedding of a graph G onto the N-node linear array with dilation d and congestion c it is trivial to obtain a normal collinear layout for G with wiring width c and longest edge of length $O(d\Delta + c)$.

In [7] it is shown how to construct normal collinear layouts for a graph G with a $f(x)$-bisector. The layout has wiring width $O(f(N)\log N)$ in general, but if $f(x) = \Omega(x^\alpha)$ for $\alpha > 0$, then the wiring width is $O(f(N))$.

For graphs with F-bifurcators we can obtain a similar result in the following lemma.

Lemma 2 *If G has a F-bifurcator, then it has a normal collinear layout with wiring width $O(F)$.*

Proof: (Sketch) We use a divide-and-conquer process that divides the graph into two subgraphs, obtains a collinear layout of each subgraph, and reconnects the two layouts by adding at most as many new rows as edges were removed in the division step. ∎

Since the process of finding good embeddings, small bisectors, or small bifurcators for an arbitrary graph is not easy in general, we present a general method to obtain a normal

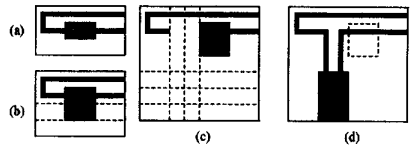

Figure 2: Transformation of a compact layout into a collinear layout.

collinear layout from an arbitrary layout.

Lemma 3 *If G has a layout of length l and with w, G also has a seminormal collinear layout of length $O(l + N\Delta)$ and wiring width $O(w)$.*

Proof: We show how to transform the given layout into a seminormal collinear layout with the claimed dimensions. The transformation is illustrated in Figure 2 for one node. Its initial appearance is shown in Figure 2.a. We first reshape the nodes by adding new rows so that each node u uses at least Δ_u rows (Figure 2.b). The width of the resulting layout is at most $O(w)$. Then, we create Δ new rows at the bottom of the layout, where all the nodes will eventually be moved (see Figure 2.c where we assumed $\Delta = 3$).

Then, the following step is applied iteratively until all the nodes are in the bottom rows and we have the desired layout. Search from left to right for the first column with tiles assigned to nodes not yet moved and take one of these nodes, say u. Create Δ_u new columns on the left side of u. When creating these columns do not stretch the wires incident to u across the columns just created (Figure 2.c). Then, move u to the bottom rows, after resizing it to $\Delta_u \times \Delta$. Finally, use the newly created columns as well as the rows previously allocated to u to reroute the edges from the bottom rows (Figure 2.d). ■

The above lemma shows that any layout can be transformed into a seminormal collinear layout with wiring width of the same order as the width of the original layout. The collinear layout obtained can now be compressed to obtain a normal collinear layout.

Lemma 4 *If G has a seminormal collinear layout with wiring width w, it also has a normal collinear layout with wiring width at most w.*

Proof: The original layout gives us a possible order in which the nodes of G can be placed to obtain the desired wiring width w. This is all we need for the purpose of obtaining the desired normal layout. We place the nodes touching each other along a straight line. We then connect these nodes by three-segment wires (two vertical and one horizontal) as defined by the original layout. This yields the desired layout. ■

Note that, in the above obtained layout, the length of the longest wire is at most $2w+\Delta c$, where c is the maximum distance between two connected nodes.

4.3.2: The layout method for product graphs: The following theorem gives an algorithm to obtain the layouts for a product graph from a normal collinear layout of its factor graph.

Theorem 6 *If G has a normal collinear layout with wiring width w, then PG_r has a layout with square nodes of side $\Delta\lceil r/2\rceil$, placed regularly in $N^{\lceil r/2\rceil}$ columns of $N^{\lfloor r/2\rfloor}$ nodes each, where two adjacent columns of nodes are at a distance of $w\sum_{i=0}^{\lfloor r/2\rfloor-1} N^i$ and two adjacent rows of nodes are at distance $w\sum_{i=0}^{\lceil r/2\rceil-1} N^i$.*

Proof: We show the iterative process that is used. Figure 3 illustrates the proof. Figure 3.a is a normal collinear layout for the 2-node linear array.

Initially, we place the N^r nodes touching each other as squares of side $\Delta\lceil r/2\rceil$ in a grid

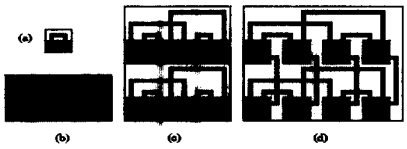

Figure 3: Layout for the 3-dimensional hypercube.

Factor network	Lower bounds	Upper bounds			
		Bisector ($r = 2$)	Bisector ($r > 2$)	Bifurcator	Collinear
Linear array	$\Omega(N^{2(r-1)})$	$O(N^2 \log^2 N)$	$O(N^{2(r-1)})$ *	$O(N^{2(r-1)} \log^2 N \log^2(\frac{N}{\log N}))$	$O(N^{2(r-1)})$ *
C. binary tree	$\Omega(N^{2(r-1)})$	$O(N^2 \log^2 N)$ *	$O(N^{2(r-1)})$ *	$O(N^{2(r-1)} \log^2 N \log^2(\frac{N}{\log N}))$	$O(N^{2(r-1)} \log^2 N)$
Shuffle-Exch.	$\Omega(\frac{N^{2r}}{\log^2 N})$	UN	UN	$O(\frac{N^{2r} \log^2 \log N}{\log^2 N})$	$O(N^{2r}/\log^2 N)$ *
de Bruijn	$\Omega(\frac{N^{2r}}{\log^2 N})$	UN	UN	$O(\frac{N^{2r} \log^2 \log N}{\log^2 N})$	$O(N^{2r}/\log^2 N)$ *
Butterfly	$\Omega(\frac{N^{2r}}{\log^2 N})$	$O(N^4)$	$O(\frac{N^{2r}}{\log^2 N})$ *	$O(\frac{N^{2r} \log^2 \log N}{\log^2 N})$	$O(N^{2r}/\log^2 N)$ *
CCC	$\Omega(\frac{N^{2r}}{\log^2 N})$	$O(N^4)$	$O(\frac{N^{2r}}{\log^2 N})$ *	$O(\frac{N^{2r} \log^2 \log N}{\log^2 N})$	$O(N^{2r}/\log^2 N)$ *
Hypercube	$\Omega(2^{2(r-1)})$	N.A.	N.A.	N.A.	$O(2^{2(r-1)})$ *
K_N	$\Omega(N^{2(r+1)})$	N.A.	N.A.	N.A.	$O(N^{2(r+1)})$ *

Table 1: Bounds on the layout area obtained for several networks by application of the presented methods. UN stands for "unknown", N.A. stands for "not applicable". The upper bounds marked with "*" are optimal.

fashion with $N^{\lceil r/2 \rceil}$ columns of nodes and $N^{\lfloor r/2 \rfloor}$ rows of nodes (Figure 3.b). The size of the nodes guarantees enough connection points in each node.

For each row of nodes we apply the following iterative process, for $i = 1...\lceil r/2 \rceil$. We start by creating wN^{i-1} new rows above the nodes. We divide the nodes in $N^{\lceil r/2 \rceil - i}$ groups of N^i adjacent nodes each. Then, we divide the group in sets of N nodes, N^{i-1} nodes apart from one another, and connect the sets as defined by the normal collinear layout using the created rows. The total number of wiring rows created is $w \sum_{i=0}^{\lceil r/2 \rceil - 1} N^i$ (Figure 3.c). This is the distance between two rows of processors.

The same iterative process can be applied to connect the columns (Figure 3.d). Then, the columns of processors are at a distance of $w \sum_{i=0}^{\lfloor r/2 \rfloor - 1} N^i$. This completes the proof. ■

From this theorem we can obtain bounds for the layout as follows:

Corollary 3 *If G has a normal collinear layout with wiring width w, where two connected nodes are at most c nodes apart, then PG_r can be laid out in an area of dimensions $\Theta(wN^{r-1}) \times \Theta(wN^{r-1})$ with maximum wire length $\Theta(cwN^{r-2})$.*

Proof: The length of the layout obtained from the above theorem along the horizontal dimension is $N^{\lceil r/2 \rceil}(\Delta\lceil r/2 \rceil + w \sum_{i=0}^{\lfloor r/2 \rfloor - 1} N^i)$. Since $w \geq \Delta/2$, $\sum_{i=0}^{\lfloor r/2 \rfloor - 1} N^i = \Theta(N^{\lfloor r/2 \rfloor - 1})$, and $N^{\lfloor r/2 \rfloor - 1} \geq \lceil r/2 \rceil$ for $N \geq 2$ and $r \geq 2$, then this length is $\Theta(wN^{r-1})$. The length along the vertical dimension is $N^{\lfloor r/2 \rfloor}(\Delta\lceil r/2 \rceil + w \sum_{i=0}^{\lceil r/2 \rceil - 1} N^i) = \Theta(wN^{r-1})$. Similarly, the length of the longest edge is at most $2w \sum_{i=0}^{\lceil r/2 \rceil - 1} N^i + b(N^{\lceil r/2 \rceil - 1}(\Delta\lceil r/2 \rceil + w \sum_{i=0}^{\lfloor r/2 \rfloor - 1} N^i)) = \Theta(bwN^{r-2})$. ■

5: Conclusions and comparison of results

In this paper we have investigated bounds on the area and wire length of layouts for homogeneous product networks. We have obtained lower bounds based on the maximal

Factor network	Lower bounds	Upper bounds			
		Bisector ($r=2$)	Bisector ($r>2$)	Bifurcator	Collinear
Linear array	$\Omega(N^{r-2}/r)$	$O(\frac{N \log N}{\log \log N^2})$	$O(N^{r-1})$	$O(N^{r-1} \log N \frac{\log(N/\log N)}{\log \log \log N})$	$O(N^{r-2})$ *
Compl. binary tree	$\Omega(\frac{N^{r-1}}{r \log N})$	$O(\frac{N \log N}{\log \log N^2})$	$O(N^{r-1})$	$O(N^{r-1} \log N \frac{\log(N/\log N)}{\log \log \log N})$	$O(N^{r-1} \log N)$
Shuffle-Exch.	$\Omega(\frac{N^r}{r \log^2 N})$	UN	UN	$O(N^r \frac{\log \log N}{\log N \log \log \log N})$	$O(\frac{N^r}{\log^{3/2} N})$
de Bruijn	$\Omega(\frac{N^r}{r \log^2 N})$	UN	UN	$O(N^r \frac{\log \log N}{\log N \log \log \log N})$	$O(\frac{N^r}{\log^{3/2} N})$
Butterfly	$\Omega(\frac{N^r}{r \log^2 N})$	$O(N^2)$	$O(N^r)$	$O(N^r \frac{\log \log N}{\log N \log \log \log N})$	$O(\frac{N^r}{\log^2 N})$ *
CCC	$\Omega(\frac{N^r}{r \log^2 N})$	$O(N^2)$	$O(N^r)$	$O(N^r \frac{\log \log N}{\log N \log \log \log N})$	$O(\frac{N^r}{\log^2 N})$ *
Hypercube	$\Omega(2^{r-2}/r)$	N.A.	N.A.	N.A.	$O(2^{r-2})$ *
K_N	$\Omega(N^{r+1}/r)$	N.A.	N.A.	N.A.	$O(N^{r+1})$ *

Table 2: Bounds on the wire length obtained for several networks by application of the presented methods. UN stands for "unknown", N.A. stands for "not applicable". The upper bounds marked with "*" are optimal if r is bounded.

congestion of the factor network, and upper bounds based on the existence of a bisector, a bifurcator, or an efficient normal collinear layout for the factor graph.

A comparison of the area bounds for some product networks is given in Table 1. The method based on collinear layouts generates optimal area layouts in most of the cases. The layouts obtained by using bisectors (when applicable) are also quite area efficient, since they have optimal area for more than two dimensions. However, we want to note that the cases where bisectors have been applied are very simple. The layouts obtained by using bifurcators are not area optimal, but are off by only a polylogarithmic function of N. In Table 2 we compare the results of wire length. If r is bounded, the collinear method is optimal in most cases. For the other cases it gives better bounds than the other two approaches.

The above analysis suggest the method based on collinear layouts as a very useful and powerful approach to the layout problem for homogeneous product networks. More research may help in finding normal collinear layouts with small wiring width for a variety of factor graphs. Clearly, it is still necessary to study how to extend these results for heterogeneous product networks.

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